A 50 MHz-30 GHz Broadband Co-Planar Waveguide SPDT PIN Diode Switch with 45-dB Isolation

Kevin W. Kobayashi, *Member, IEEE*, Liem Tran, Aaron K. Oki, *Member, IEEE*, and Dwight C. Streit, *Member, IEEE*

***Abstract*— This paper reports on a GaAs PIN diode SPDT switch design which achieves 45 dB of isolation up to 30 GHz. The switch design uses 2-μm-thick i-region PIN's, a shunt-shunt-series switch topology in each arm, and a quasi-coplanar waveguide (CPW) design environment to achieve its superior isolation performance. By employing CPW ground isolation with a microstrip design, as much as 10-dB improvement in isolation performance was observed at the upper band frequencies. The switch achieves 1.02-dB insertion loss and >15-dB input and output return-loss across the band. In comparison to previously reported GaAs MMIC PIN diode switches at millimeter-wave frequencies, this design achieves state-of-the-art isolation performance.**

I. Introduction

HIGH IP3 broadband switches are important for EW and communication systems. PIN diode switches are often chosen for their high IP3 and high power handling capability as well as their high frequency of operation. The GaAs PIN's reported in this work achieve cutoff frequencies of >1.6 THz which is comparable to previously reported GaAs PIN diodes [1]–[5]. This work describes the design of a broadband 30-GHz quasi-CPW SPDT PIN diode switch and compares its measured performance with an equivalent conventional microstrip switch design.

II. Switch Design

One very important performance parameter which is sensitive to both design and PIN diode device characteristics is the off-isolation. This parameter is sometimes considered to be the most difficult to achieve because it is dependent on many factors. The off-isolation is limited by the PIN diode series on-resistance and off-capacitance. PIN diodes with large on-resistance/off-capacitance cutoff frequencies ($f_c = 1/[2\pi R_{\rm on}\ C_{\rm off}]$) result in superior switch performance. In addition, the PIN switch design topology greatly affects the isolation performance. Two shunt diodes and one series diode is used in each arm of the SPDT switch of this work in order to achieve good isolation performance. The two shunt PINs ensure good isolation between the two rf paths of the switch. This topology maximizes isolation while minimizing insertion loss and has previously achieved >42 dB of isolation up to 20 GHz [1]. For frequencies >20 GHz (millimeter-wave), electromagnetic coupling between switch arms can limit the isolation performance. The design presented in this work employs a coplanar ground on the top of the GaAs substrate to reduce radiation coupling and improve the isolation between the arms of the microstrip switch.

Manuscript received September 13, 1994.

The authors are with TRW Electronics Systems and Technology Division, One Space Park, Redondo Beach, CA 90278 USA.

IEEE Log Number 9407740.

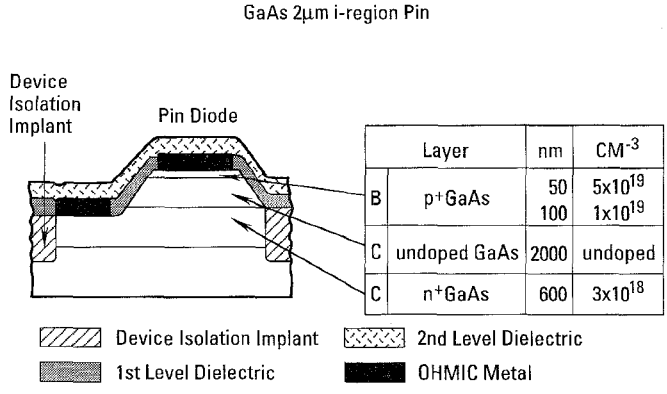


Fig. 1. Molecular beam epitaxy profile of the 2-μm PIN diode structure.

The GaAs PIN diodes used in the switch design are based on our previously reported HBT MBE profile which has produced X-band SPDT PIN switches, attenuators, and variable gain amplifiers [2]. The PIN diodes described in the present work differ in MBE structure in two counts: 1) the lightly doped n^- collector region is now undoped GaAs ($\approx 10^{14}$ cm^{-3}), and 2) the undoped i-region is now 2000 nm thick (increased from 700 nm). The MBE profile illustrating the resulting PIN diode structure is shown in Fig. 1. For our switch designs, 9-μm-radius (p-ohmic) PIN diodes were used. The on-resistance of this size diode is 3.7 Ω and the off-capacitance under reverse bias is 27 fF. The corresponding on-resistance/off-capacitance cutoff frequency is 1.6 THz.

The SPDT switch was first designed in a microstrip environment using small-signal simulations. Then CPW ground planes were added to the circuit, and were modeled using the CPW models in LIBRA. The CPW center conductor line widths and lengths were left the same as in the original microstrip design. The CPW spacing was chosen to be 35 μm, large enough to minimize the CPW effect on the microstrip rf performance, and small enough to accommodate airbridge jumpers to provide ground continuity and inhibit waveguide moding effects. In addition, backside vias were used to connect the CPW ground with the backside ground. The backside vias were strategically placed along the arms of the switch in order to inhibit extraneous coupling through the GaAs substrate.

III. Measured Results

Fig. 2 shows a photograph of the fabricated 50 MHz-30 GHz PIN diode switch with coplanar waveguide isolation. The

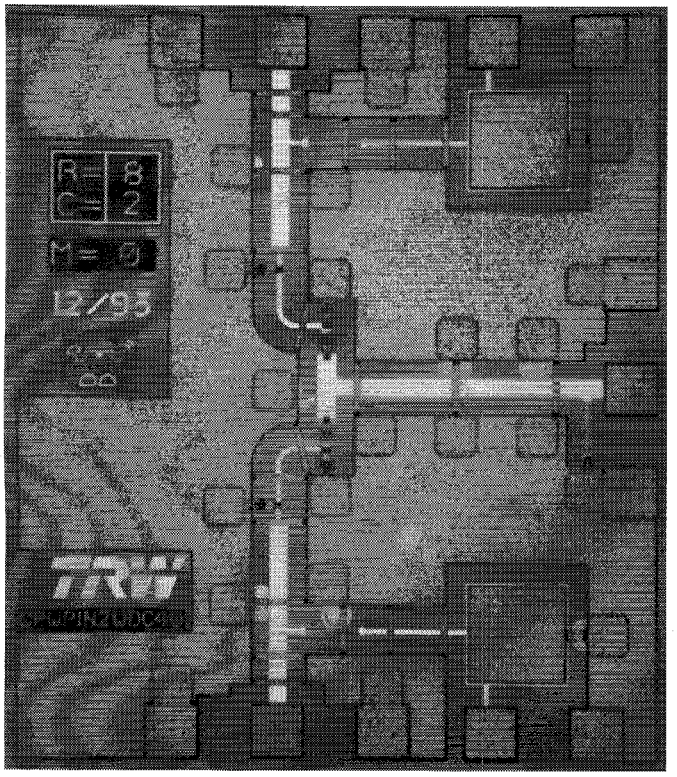
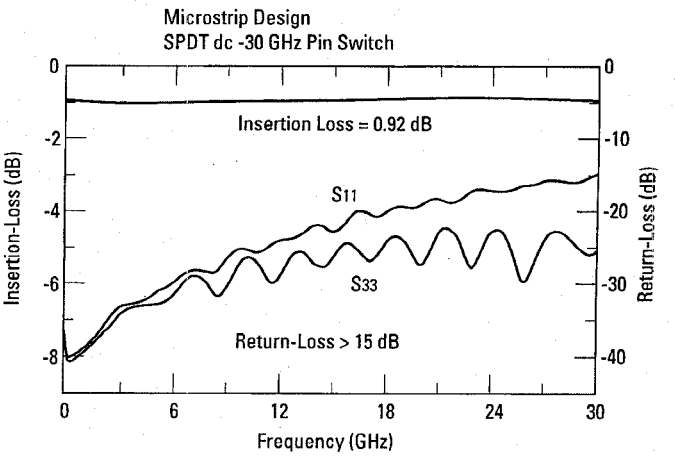


Fig. 2. Micro-photograph of the fabricated SPDT microstrip design with CPW ground isolation. The chip size is 1.3×1.5 mm^2.

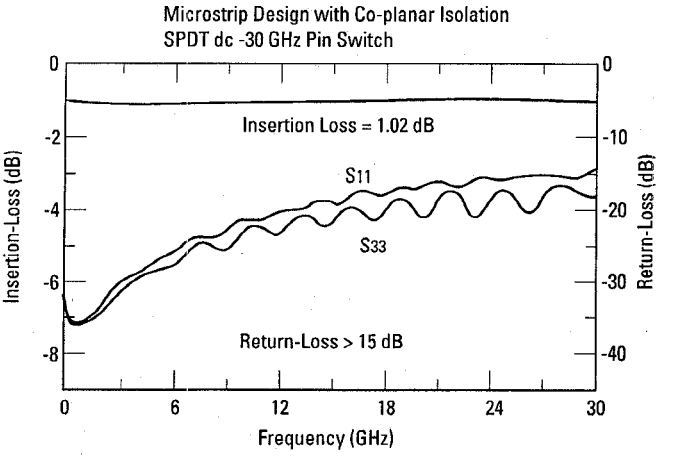
chip is 1.3×1.5 mm^2 in area. An identical chip (not shown) without the CPW ground planes was also fabricated for performance comparison. When one arm is switched on, the supply voltage is $+1.24$ V with as little as 5 mA of bias current. The other complementary arm is biased with -10.3 V and a bias current of 9.35 mA. Under this bias condition, each of the shunt diodes are forward biased at 4.7 mA, and the series diode is reversed biased with -5.3 V. Fig. 3(a) and 3(b) shows the respective insertion-losses and return-losses of the two designs. The conventional microstrip design achieves an insertion-loss of 0.92 dB across the 0.05–30 GHz band, and input/output return-losses >15 dB. The microstrip design with coplanar isolation achieves 1.02-dB insertion loss and the input/output return-losses are also >15 dB. The isolation performance of the two designs were measured and are shown for comparison in Fig. 4. The conventional microstrip design achieves an average isolation of 35 dB while the design employing the additional CPW ground achieves an average isolation of 45 dB across the band. Thus, as much as 10-dB improvement in isolation performance was observed up to 30 GHz for the design employing coplanar ground isolation. We believe this improvement will begin to decrease at higher frequencies (>40 GHz) where the finite PIN diode off-capacitance begins to heavily influence the isolation performance. In general, the limitation of this technique is dependent on the performance of the PIN diode used in the design.

IV. Conclusion

A SPDT PIN diode microstrip design with CPW ground for improved isolation was demonstrated with 45-dB isolation performance from 0.05 MHz to 30 GHz. Employing a CPW ground resulted in as much as 10-dB improvement in isolation performance at millimeter-wave frequencies over a conventional microstrip design without the CPW grounding. This experimental result indicates that a switch designed in a CPW environment can significantly enhance switch isolation performance at millimeter wave frequencies.



(a)



(b)

Fig. 3. Insertion-loss and return-loss performance of (a) the conventional microstrip design, and (b) the microstrip design with CPW ground isolation.

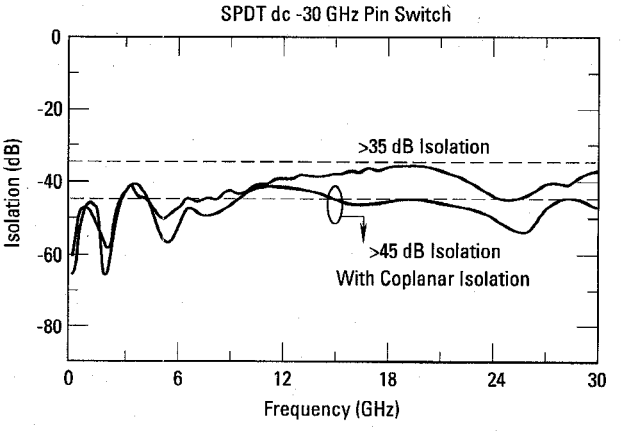


Fig. 4. Isolation performance of the conventional and CPW isolated designs.

ACKNOWLEDGMENT

The authors would like to thank B. Nelson, Drs. W. Jones and F. Oshita for the initial development work on the 2-μm GaAs PIN diodes, L. Sjogren for discussions on switch isolation techniques, and T. Naeole for processing.

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